Zynq All Programmable SoC System Architecture + Embedded S/W design

Embedded Architect 3

EMBD24000-ILT- Vai

Course Specification

Course Description

The Xilinx Zynq® System on a Chip (SoC) + Embedded Software design provides a new level of system design capabilities. This course provides system architects with the knowledge to effectively architect a Zynq All Programmable SoC and implement embedded software solutions.

This course presents the features and benefits of the Zynq architecture for making decisions on how to best architect a Zynq All Programmable SoC project. It covers the architecture of the ARM® Cortex™-A9 processor-based processing system (PS) and the connections to the programmable logic (PL) at a sufficiently deep level that a system designer can successfully and effectively utilize the Zynq All Programmable SoC.

The course details the individual components that comprise the PS: I/O peripherals, timers, caching, DMA, interrupt, and memory controllers. Emphasis is placed on effective access and usage of the PS DDR controller from PL user logic, efficient PL-to-PS interfacing, and design techniques, tradeoffs, and advantages of implementing functions in the PS or the PL.

Level –Intermediate

Course Duration – 3 days

Price –

Course Part Number – EMBD24000-ILT- Vai

Who Should Attend? – System architects who are interested in architecting a system on a chip using the Zynq All Programmable SoC and interested in learning about the embedded software enabling techniques for Zynq design..

Prerequisites

- Digital system architecture design experience
- Basic understanding of microprocessor architecture
- Basic understanding of C programming
- Basic HDL modeling experience

Software Tools

- Vivado® Design or System Edition 2014.3

Hardware

- Architecture: Zynq-7000 All Programmable SoC*
- Demo board: Zynq-7000 All Programmable SoC ZC702 or Zed board*

This course focuses on the Zynq-7000 All Programmable SoC. Check with your local Authorized Training Provider for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Describe the architecture and components that comprise the Zynq All Programmable SoC processing system (PS)
- Relate a user design goal to the function, benefit, and use of the Zynq All Programmable SoC
- Effectively select and design an interface between the Zynq PS and programmable logic (PL) that meets project goals
- Analyze the tradeoffs and advantages of performing a function in software versus PL

Course Outline

Day 1

- Zynq All Programmable SoC Overview
- Inside the Application Processor Unit (APU)
- Processor Input/Output Peripherals
- **Lab 1:** Building a Zynq All Programmable SoC Platform
- Process Input/Output Peripherals
- Introduction to AXI
- Zynq All Programmable SoC PS/PL AXI Ports
- **Lab 2:** Integrating Programmable Logic on the Zynq All Programmable SoC
- Zynq All Programmable SoC Booting

Day 2

- Zynq All Programmable SoC Memory Resources
- Meeting Performance Goals
- **Lab 3:** Using DMA on the Zynq All Programmable SoC
- Zynq All Programmable SoC Hardware Design
- Debugging the Zynq All Programmable SoC
- **Lab 4:** Debugging on the All Programmable SoC
- Processors, Peripherals and Tools
- Standalone Software Platform Development
- **Lab 5:** Running a Linux App on the Zynq All Programmable SoC

Day 3

- Linux Software Application Development
- Software Development Using SDK
- Writing Code in the Xilinx Standalone Environment
- Writing Code in the Xilinx Linux Environment
- **Lab 6:** Application Development (Standalone or Linux)
- Demo: SDK Batch Mode
- Address Management
- Interrupts
- **Lab 7** Software Interrupts
- Software Platform Download and Boot
- Application Debugging
- **Lab 8:** Debugging or Linux Debugging

Appendix

- Application Profiling
- **Lab A:** SDK Profiling
- Writing a Custom Device Driver
- **Lab B:** Writing a Device Driver
- Advanced Services and Operating Systems
- Project Management with the Xilinx Design Tools
- **Lab C:** File Systems

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Lab Descriptions

- **Lab 1:** Building a Zynq All Programmable SoC Platform – Examine the process of using the Vivado IP Integrator tool to create a simple processing system.
- **Lab 2:** Integrating Programmable Logic on the Zynq All Programmable SoC – Connect a programmable logic (PL) design to the embedded processing system (PS).
- **Lab 3:** Using DMA on the Zynq All Programmable SoC – Experiment with effectively using the PS DMA controller to move data between DDRx memory and a custom PL peripheral.
- **Lab 4:** Debugging on the Zynq All Programmable SoC – Evaluate debugging the hardware and software components of a Zynq All Programmable SoC design.
- **Lab 5:** Running a Linux App on the Zynq All Programmable SoC – Create a simple hello_world application using the SDK.
- **Lab 6:** Application Development (Standalone or Linux - Create a simple software application project with the provided source files for a software loop-based stopwatch; or, access the general-purpose input/output (GPIO) that is connected to the evaluation board.
- **Lab 7:** Software Interrupts - Replace a software timing loop with an interrupt-driven timer. Add the timer software and implement an interrupt handler for the timer.
- **Lab 8:** Debugging (Standalone or Linux) - Launch the SDK debug perspective and the Lab 6 or Lab 7 application for debugging, setting breakpoints, calculating interrupt latency, and stepping through the program's operation.

Register Today by contacting: info@vailogic.com

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